SiO_2 is amorphous

US-PAT-NO: 5825068

DOCUMENT-IDENTIFIER: US 5825068 A

TITLE: Integrated circuits that include a barrier layer reducing hydrogen
diffusion into a polysilicon resistor

---------- KWIC ---------

In order to increase the number of dangling bonds, in some embodiments the
barrier layer includes multiple layers of polysilicon or amorphous silicon that
are separated by thin layers of silicon dioxide. Silicon dioxide is an
amorphous material, and silicon grains do not extend across the silicon
dioxide. Consequently, the silicon grain vertical dimension is reduced. Of
note, some polysilicon deposition techniques produce silicon grains that extend
vertically (have columnar structure). See S. Wolf, et al., "Silicon Processing
for the VLSI Era; Volume 1--Process Technology" (1986), pp. 179-180. The
silicon dioxide limits the vertical extent of these columnar grains.

5057897 19911000 Nariani et al. 257/637

5336335 19940800 Hall et al. 257/51

5349325 19940900 McAllister 257/536

5374833 19941200 Nariani et al. 257/52

5457335 19951000 Kuroda et al. 257/318

SiO_2 is amorphous

US-PAT-NO: 5248564

DOCUMENT-IDENTIFIER: US 5248564 A

TITLE: C-axis perovskite thin films grown on silicon dioxide

---------- KWIC ---------

Nonetheless, depositing a buffer layer of YSZ on silicon prior to forming the ferroelectric elements is not totally satisfactory. The silicon substrate is advantageous in that silicon support circuitry, especially complementary metal-oxide-semiconductor (CMOS) circuitry, can be fabricated in it. The YSZ is deposited at a temperature around 800.degree. C., which is incompatible with silicon CMOS processing. It would be especially advantageous if the ferroelectric elements could be grown on silicon dioxide, which is an amorphous glass. The silicon oxide would isolate the ferroelectric elements and could be used as the oxide layer in a metal-oxide-semiconductor (MOS) gate transistor associated with each ferroelectric memory cell. Unfortunately, LSCO grown directly on SiO.sub.2 shows very little crystallographic orientation and appears to be polycrystalline. Also, PZT grown directly on the SiO.sub.2 forms in the non-ferroelectric pyrochlore phase.

DRAMs comprise a plurality of (pairs apart WL, which comprises the gate structures.

US-PAT-NO: 5864496

DOCUMENT-IDENTIFIER: US 5864496 A

TITLE: High density semiconductor memory having diagonal bit lines and dual word lines

---------- KWIC ---------

Conventional DRAM chips employ millions of memory cells arranged in one or more arrays of rows and columns, with bit lines running parallel to the columns and word lines running parallel to the rows. Each memory cell is comprised of an access transistor (e.g., an NFET) and a capacitor such as a trench capacitor for storing charge corresponding to a data bit. The memory cells are typically located at the intersections of the word lines and bit lines. The gate electrode of each access transistor is electrically connected to the associated word line while the transistor's drain terminal is connected to the associated bit line.

US-PAT-NO: 5576223

DOCUMENT-IDENTIFIER: US 5576223 A

TITLE: Method of defect determination and defect engineering on product wafer of advanced submicron technologies

---------- KWIC ---------

Referring now to FIG. 1, there is shown a sectional view of a portion of an integrated circuit 10 which can be made by a process developed in accordance with a method of the present invention. Integrated circuit 10 typically contains a plurality (e.g., 64 million) of switched capacitor memory cells (only one of which is shown) which form a dynamic random access memory (DRAM). Integrated circuit 10 comprises a body 12 of a semiconductor material, such as single crystalline silicon, having a surface 14. A relatively narrow, deep trench 16 extends into the body 12 from the surface 14. A wider but shallower trench 18 extends into the body 12 from the surface 14 adjacent one side of the deep trench 16. The wall of the deep trench 16 is covered with a thin layer 20 of a dielectric material, typically silicon dioxide. The remaining portion of the deep trench 16 is filled with a body 22 of conductive polycrystalline silicon. The polycrystalline silicon body 22 and the silicon body 12 serve as the plates of a capacitor with the dielectric layer 20 therebetween. The shallow trench 18 is filled with an insulating material 24, typically silicon dioxide, to serve as an isolation means.

US-PAT-NO: 5471421

DOCUMENT-IDENTIFIER: US 5471421 A

TITLE: Storage cell using low powered/low threshold CMOS pass transistors
having reduced charge leakage

---------- KWIC ---------

Dynamic random access memories (DRAMs) and static random access memories
(SRAMs) typically include a number of storage cells that are organized in
arrays having a plurality of rows and columns. In both DRAMs and SRAMs, a word
line is associated with each row in the array. In DRAMs, one bit line is
associated with each column in the array. With SRAMs, differential bit lines
are associated with each column in the array. The reading or writing of a
particular cell or row of cells in both DRAMs and SRAMs is performed using
decoders, sense amplifiers, multiplexer circuits, write drivers, etc., in a
well known manner, and is therefore not explained in greater detail herein.

US-PAT-NO: 5945704

DOCUMENT-IDENTIFIER: US 5945704 A

TITLE: Trench capacitor with epi buried layer

---------- KWIC ---------

Referring to FIG. 1, a conventional trench capacitor DRAM cell 100 is shown.
Such a conventional trench capacitor DRAM cell is described in, for example,
Nesbit et al., A 0.6 .mu.m.sup.2 256 Mb Trench DRAM Cell With Self-Aligned
Buried Strap (BEST), IEDM 93-627, which is herein incorporated by reference for
all purposes. Typically, wordlines and bitlines interconnect a plurality of
memory cells, forming a cell array in a DRAM chip.

US-PAT-NO: 6477081

DOCUMENT-IDENTIFIER: US 6477081 B2

TITLE: Integrated memory having memory cells with a magnetoresistive storage property

---------- KWIC ---------

Integrated memories having memory cells of this type, also referred to as MRAMs (Magnetoresistive Random Access Memory), are often of a similar structure to that of, for example, integrated memories of the DRAM (Dynamic Random Access Memory) type. Memories of this type generally have a memory cell configuration with row lines and column lines which run essentially parallel to one another, with the row lines usually running transversely with respect to the column lines.